<table>
<tr><td>ESRF</td><td>Experiment title:
A detailed study of the effect of grain structure on stress and stress evolution in sub-micron interconnects</td><td>Experiment number:
MA1071</td></tr>
<tr><td>Beamline:
ID01</td><td>Date of experiment:
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Received at ESRF:</td></tr>
<tr><td>Shifts:
12</td><td>Local contact(s):
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Report:

Our previous work suggetsed that grain structure can play an important role in defining the stress and stress evolution in interconnect structures. As interconnect dimensions are scaled, interconnects will become more sensitive to these effects; with limitations in copper plating chemistries causing divergent grain structures across a chip, compounded with increasing aspect ratios to lower line resistance restricting grain boundary mobility in trenches. The purpose of this work was to utilise high resolution and focused X-rays to directly study the tri-axial stress in scaled microelectronic circuit interconnects and correlate this to grain structure. Samples fabricated in imec, with line width sclaed below 45nm were tested.

Publications on the results outlined below are in-preparation or submitted at the time of preparing this report.

Using two students on shifts we managed to run samples for an average of 20+ hours day. This beam time was scheduled prior to MA1070 which had similar goals so the time was split between the two experiments to make the most the beam down day in the middle.

At the start of this beam time we were affected by focusing problems as the slits and detector used previously were not available. After some time optimising the availabe set up, the diffraction peak shape we obtained previously could not be obtained. Selected measurements were started using the available set up, however the resolution in Bragg peak position could not be obtained. In hindsight, also a higher beam energy was used compared to our previous work, lowering the Bragg angle, and contributing to the lower resolution in peak position. This should be improved next time.

To make use of the time, additional measurements were made on blanket relavent to the semiconductor industry samples where the peak resolution was not critical. TiO2 and Al doped TiO2 films grown on oxidized Ru as deposited at 250°C or after 400°C post-deposition anneal in Ar were measured. Figure 1 shows a structural change that occurs only for the annealed TiO2 films. In these films, the appearance of additional peaks (marked by ↓) are likely due to the formation of titanium sub-oxides TiO2-x due to generation of oxygen vacancies. In the case of Al doped TiO2, no change in the layer structure has occurred likely, due to neutrality of the structure as Al3+ can compensate the appearance of oxygen vacancies. The increase in leakage current density that take place after anneal only in the TiO2 layers is explained by formation of oxygen vacancies.

(a) (b)

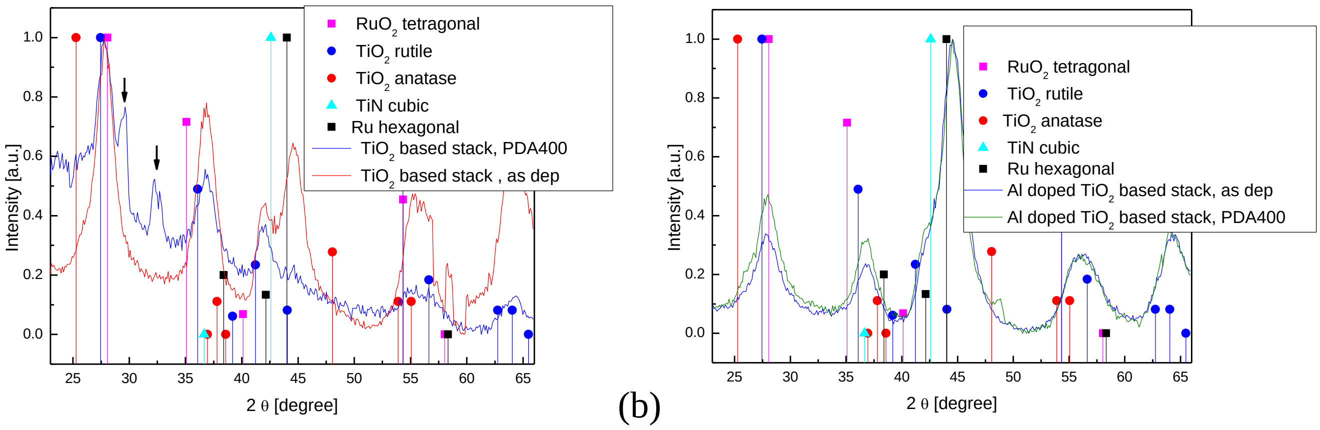

Figure 1. GID of TiO2 based stack (a) and Al doped TiO2 based stack (b) as deposited at 250°C and after post-deposition anneal at 400°C.

After new/fixed detector slits were available, measurements on the patterned interconnect samples could continue. The typical stack used for all measurements is shown in figure 2.

(a) (b)

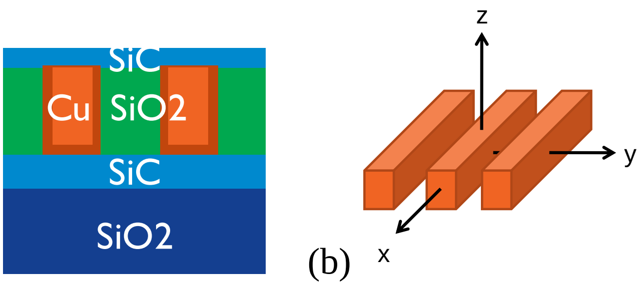

Figure 2. (a) Typical stack used for stress measurements and (b) Co-ordinate system

Tri-axial stress measured as a function of post plating anneal time shows stress relaxation indicative of grain growth and reorder in a polycrystalline line (fig 3a). A high temperature sinter step continues to reduce in-plane stress but increases out of plane stress (fig. 3b). The stress in narrow lines with different grain structures was further investigated with other samples. Three samples were produced with different grain structures. Based on transmission electron microscopy (TEM) and grain boundary detection software sampling over 200 grains, samples were classified as: A "semi-bamboo" (a mixture of single and multi grains in the line width); B "polycrystalline" (multiple grains in line width); and C "bamboo" (one grain across line with). Figure 4 shows the hydrostatic stress for these samples before and after annealing. This shows as bamboo lines are constrained in their width, stress cannot be relieved with thermal treatments, and stress increases (sample C). More polycrystalline lines are able to re-order and the stress can reduce (sample B).

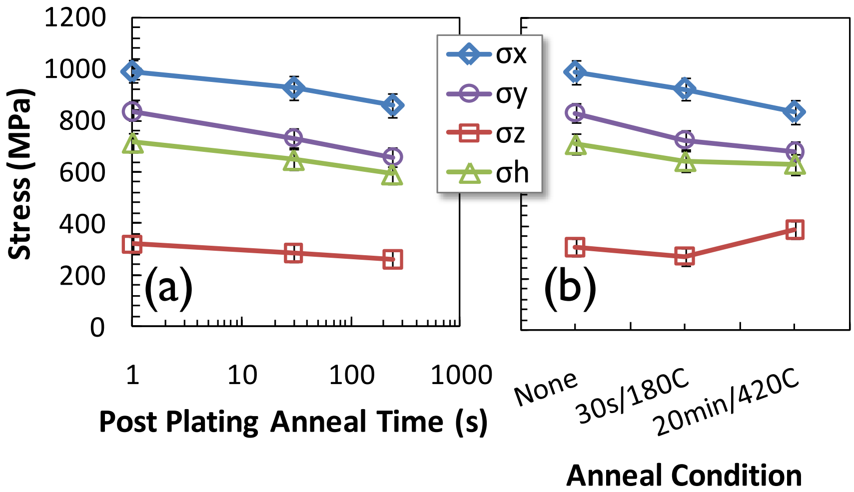

Figure 3. Cu tri-axial stress as a function of anneal (a) time and (b) condition.

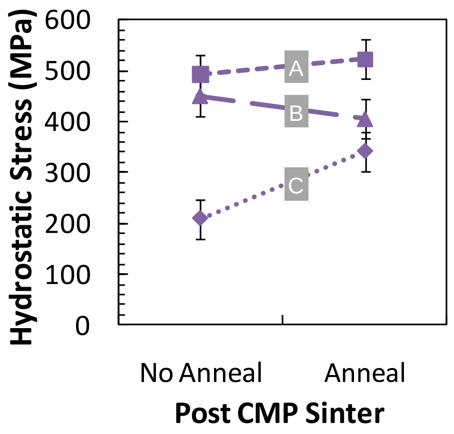

Figure 3. Hydrostatic stress for Cu lines with different grain structures before and after annealing

Finally, the effect of the various process steps used in the fabrication of the samples was studied. Figure 5a shows the stress for blanket wafers produced using different electro-chemical plating chemistries. A small difference is observable between chemistry A and B however chemistry C has intrinsically almost 100% larger in-place (σ_x) stress. Note these blanket films have no σ_y component as the Cu is in a bi-axial condition. Figure 5b shows how this changes when patterning the film. A higher stress is obtained in the bulk Cu compared to the blanket reference. Once the bulk material is removed by chemical mechanical polishing (CMP) the tri-axial stress in the Cu lines and be accessed. A significant increase in stress is observed in all tri-axial components. Figure 5c shows the effect of reduced time processing between the Cu plating step (fig 5b left) and CMP (fig 5b right). The use of reduced time between plating and CMP increases the stress suggesting self annealing may reduce the stress in the no-CTL case.

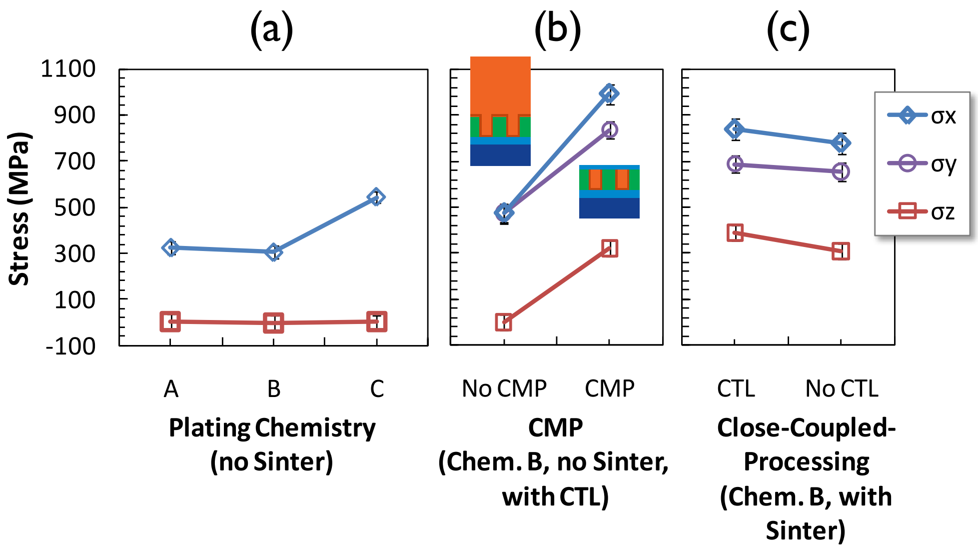

Figure 5. Tri-axial stress using different processing conditions: (a) blanket, (b) and (c) patterned